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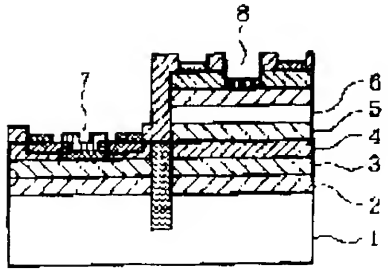
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To obtain a high-performance complementary semiconductor circuit device having a higher-speed characteristic than a silicon complementary circuit device, by simple manufacturing processes and with good reproducibility.
CONSTITUTION: A grated Si1-xGex layer 2 having an increasing Ge composition, an active layer 3 composed mainly of germanium, and a grated Si1-yGey layer 4 having a reducing Ge composition are provided on a silicon germanium substrate 1, and in its one part region a p-type transistor 7 having a silicon germanium active layer 3 as a channel layer is formed. Along with it, in an adjacent region an n-type transistor 8 is formed in a III-V compound semiconductor active layer 6 provided through the medium of a high-resistance III-V compound semiconductor layer 5.



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* NOTICES *

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by providing or including the following. The gray dead silicon germanium layer which germanium composition increases on a silicon germanium substrate, the active layer which makes germanium a principal component, and the gray dead silicon germanium layer in which germanium composition decreases. V group element is many [1 to 2%] III-V group compound semiconductor layers, and a III-V group compound semiconductor active layer to a stoichiometry to the field which adjoins the field in which this aforementioned p type transistor was prepared at least while constituting the p type transistor which uses the aforementioned silicon germanium active layer as a channel layer to a field in part. n type transistor which uses the aforementioned III-V group compound semiconductor active layer as a channel layer.
[Claim 2] The semiconductor device according to claim 1 with which the above-mentioned silicon germanium substrate, the gray dead silicon germanium layer which the above-mentioned germanium composition increases, the active layer which makes the above-mentioned germanium a principal component, and the gray dead silicon germanium layer in which the above-mentioned germanium composition decreases are characterized by having germanium composition which the misfit transition by grid mismatching does not generate.
[Claim 3] The semiconductor device according to claim 1 or 2 characterized by germanium composition of the above-mentioned silicon germanium substrate making it 0.3 or 0.7.
[Claim 4] A semiconductor device given in the claim 1 characterized by for the active layer which makes the above-mentioned germanium a principal component being a germanium active layer whose germanium composition is 100%, and the above-mentioned III-V group compound semiconductor active layer being a GaAs active layer, or any 1 term of 3.
[Claim 5] A semiconductor device given in the claim 1 characterized by for the above-mentioned p type transistor being an insulated-gate type electric field effect type transistor, and n type transistor being an HEMT, or any 1 term of 4.
[Claim 6] The gray dead silicon germanium layer which germanium composition increases on a silicon germanium substrate, The active layer which makes germanium a principal component, the gray dead silicon germanium layer in which germanium composition decreases, V group element receives a stoichiometry. Many [1 to 2%] III-V group compound semiconductor layers, And a III-V group compound semiconductor active layer is prepared. After exposing the gray dead silicon germanium layer in which the aforementioned III-V group compound semiconductor active layer and the aforementioned V group element remove alternatively many [1 to 2%] III-V group compound semiconductor layers to a stoichiometry, and germanium composition decreases. The manufacture method of the semiconductor device characterized by forming n type transistor in a III-V group compound semiconductor active-layer side while forming p type transistor in this exposed field side.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the high-speed semiconductor device of the complementary type using the III-V group compound semiconductor transistor as an n type transistor, and its manufacturing method especially about a semiconductor device and its manufacture method, using a germanium transistor as a p type transistor.
[0002]
[Description of the Prior Art] Conventionally, the high-speed performance of the complementary circuit which constitutes the base element (basic gate) of silicon semiconductor integrated circuit equipment was restricted in the property of the low p type transistor of the mobility of a carrier. For example, the hole mobility of silicon is 500cm2 / V-sec, it is about 1/3 compared with the electron mobility of 1450cm2 / V-sec, and this hole mobility had specified the property of the complementary-type semiconductor device using silicon.
[0003] In order to improve the working-speed property in such a silicon semiconductor device, the high-speed semiconductor device using III-V group compound semiconductors, such as HEMT which used GaAs as the carrier run layer, was developed, and since hole mobility was smaller than 400cm2 / V-sec, and silicon to electron mobility being 8800cm2/V-sec also in GaAs, when GaAs was used, a high-speed complementary circuit was not able to be obtained.
[0004] On the other hand as a big semiconductor of hole mobility, germanium is known, and the hole mobility is 1800cm2 / V-sec, and is about 4 times the hole mobility of silicon. In addition, the electron mobility of germanium is 3800cm2 / V-sec.
[0005] However, since there are various kinds of faults of a stable oxide film not existing in germanium and it is not realistic to constitute a complementary-type semiconductor device only using germanium, constituting a complementary circuit as an n type transistor using big GaAs of electron mobility including a circumference circuit, using germanium as a p type transistor is also proposed. Since it is n type transistor fundamentally, in case the drive system in the compound semiconductor integrated circuit device by which such a proposal included light-corpuscle children, such as OEIC, in the same substrate includes a complementary circuit in this compound semiconductor integrated circuit device, what is necessary will be to constitute only p type transistor from germanium, and it is very useful.
[0006] In this case, since the lattice constant of germanium (lattice constant : 5.6461A) and GaAs (lattice constant : 5.6533A) was very near, when a heterojunction is formed, while the problem of grid mismatching has the advantage which is not produced In order that germanium (germanium), a gallium (Ga), or arsenic (As) may work as a conductivity-type determination impurity mutually, When growing a germanium layer epitaxially on a GaAs substrate, Ga in GaAs carries out a segregation into a germanium layer, and tends to grow into p type layer. It was difficult to form the crystalline good n-type-germanium layer for constituting p type transistor, and it was difficult for counter diffusion to arise and to form a steep heterojunction on the other hand, when growing up a GaAs layer on germanium substrate.

[0007] In order to solve the problem of this segregation and counter diffusion, also making a silicon layer intervene between germanium and GaAs is proposed. (Refer to JP,5-175144,B and JP,5-259073,B) However, since germanium (lattice constant : 5.6461A) differed from GaAs (lattice constant : 5.6533A) and a lattice constant considerably, the problem of grid mismatching arose, and since the thickness which can be grown up without germanium or misfit transition on GaAs, i.e., critical thickness, became small, silicon (lattice constant : 5.4309A) was not able to suppress counter diffusion and a segregation enough in the silicon layer of the thickness below critical thickness.

[0008] Moreover, since it is necessary to make it an unstable germanium oxide film not exist in the semiconductor device which needed to avoid that germanium was exposed to air in the manufacture process, and was manufactured when a germanium substrate is used, since the oxide of germanium is water-soluble, the semiconductor device which used only germanium in addition to the special purpose is no longer used.

[0009] Furthermore, the silicon germanium (Si1-z Gez) which is the mixed crystal of silicon and germanium is also studied as another possibility for many years. Si1-z Gez Mixed crystal with zone-leveling technology Forming is proposed (J. The Journal of Physical Chemistrypvol.68 besides P.Dismukes, No.10, pp.3021-3027, Oct.1964). Moreover, recent years, This Si1-z Gez Although growing up mixed crystal by the molecular-beam epitaxial grown method (the MBE method) etc. is also studied, the exceptional concrete proposal has not accomplished. In addition, this Si1-z Gez There is a lattice constant of mixed crystal in the middle of silicon and germanium depending on a composition ratio.

[0010]

[Problem(s) to be Solved by the Invention] However, it was difficult to manufacture the highly efficient complementary-circuit equipment which has a high-speed property from conventional silicon complementary-circuit equipment in any case with repeatability to be an easy manufacturing process and sufficient. Therefore, this invention aims at obtaining the highly efficient complementary-type semiconductor circuit equipment which is an easy manufacturing process and has a high-speed property with sufficient repeatability from silicon complementary-circuit equipment.

[0011]

[Means for Solving the Problem] Drawing 1 is the cross section of the semiconductor device for explaining the theoretic composition of this invention.

The semiconductor device of the drawing 1 reference this invention on the silicon germanium substrate 1 gray dead Si1-x Gex which germanium composition increases a layer 2 and the active layer 3 which makes germanium a principal component -- and Gray dead Si1-y Gey to which germanium composition decreases Form a layer 4, and in part, while forming the p type transistor 7 which uses the silicon germanium active layer 3 as a channel layer to a field To the field contiguous to the field in which this p type transistor 7 was formed at least V group element is characterized by having formed many [1 to 2%] high resistance III-V group compound semiconductor layers 5, and the III-V group compound semiconductor active layer 6 to the stoichiometry, and forming n type transistor 8 which uses this III-V group compound semiconductor active layer 6 as a channel layer.

[0012] Moreover, this invention is the silicon germanium substrate 1 and gray dead Si1-x Gex which germanium composition increases. A layer 2, the active layer 3 which makes germanium a principal component, and gray dead Si1-y Gey to which germanium composition decreases A layer 4 is characterized by having germanium composition relation which the misfit transition by grid mismatching does not generate.

[0013] Moreover, this invention is characterized by setting germanium composition of a silicon germanium substrate to 0.3-0.7. Moreover, even if there are few p type transistors, a channel layer is germanium, and this invention is characterized by a channel layer being [of n type transistor] GaAs at least.

[0014] Moreover, this invention is characterized by using an HEMT (HEMT) as an n type transistor, using an insulated-gate type electric field effect type transistor (IGFET) as a p type transistor.

[0015] The manufacture method of the semiconductor device of this invention moreover, on the silicon germanium substrate 1 gray dead Si1-x Gex which germanium composition increases a layer 2 and the active layer 3 which makes germanium a principal component -- and gray dead Si1-y Gey to which germanium composition decreases a layer 4 and V group element -- a stoichiometry -- receiving -- many [1 to 2%] high resistance III-V group compound semiconductor layers 5 -- and Gray dead Si1-y Gey to which the III-V group compound semiconductor active layer 6 is formed, this III-V group compound semiconductor active layer 6 and V group element remove alternatively many [1 to 2%] high resistance III-V group compound semiconductor layers 5 to a stoichiometry, and germanium composition decreases A layer 4 is exposed. While forming p type transistor 7 in this exposed field side, it is characterized by forming n type transistor 8 in the III-V group compound semiconductor active-layer 6 side.
[0016]
[Function] Drawing 2 is drawing showing correlation of the germanium composition z in silicon germanium (Si1-z Gez), and a lattice constant, and explains an operation with reference to drawing 2 . As shown in drawing 2 reference drawing 2 , it is Si1-z Gez. A lattice constant increases linearly with the increase in the composition z of germanium, and carries out abbreviation coincidence with the lattice constant (lattice constant : 5.6533A) of GaAs in the pure germanium (lattice constant : 5.6461A) of x= 1.0.
[0017] Since an unstable germanium oxide film does not exist compared with the case where the problem of the grid mismatching of the active layer which makes a principal component the germanium grown up on it as a substrate since silicon germanium mixed crystal with a near lattice constant is used for germanium or GaAs rather than silicon, and a III-V group compound semiconductor active layer did not produce this invention, and a germanium substrate is used, reliability increases. Moreover, since V group element is making many [1 to 2%] III-V group compound semiconductor layers of high resistance intervene to a stoichiometry, electric separation with p type transistor and n type transistor becomes certain.
[0018] Moreover, gray dead Si1-x Gex from which germanium composition increases a substrate and germanium between the active layers made into a principal component Gray dead Si1-y Gey to which germanium composition which forms germanium the active layer made into a principal component and on it since the layer is prepared decreases The mistake foot transition by grid mismatching is not generated in a layer.
[0019] Moreover, gray dead Si1-y Gey to which germanium composition for preventing counter diffusion decreases as a substrate since germanium composition uses the silicon germanium of 0.3-0.7 A layer can be formed thickly, therefore counter diffusion with germanium, Ga, or As is suppressed effectively, and the crystallinity of a III-V group compound semiconductor layer established on it improves.
[0020] Moreover, the transistor which is a transistor which has the process established as a simple substance, and is the same unipolar mold can constitute a complementary circuit by using an HEMT (HEMT) as an n type transistor, using an insulated gate field effect transistor (IGFET) as a p type transistor.
[0021] Moreover, since V group element by low-temperature growth has combined the growth process of many [1 to 2%] high resistance III-V group compound semiconductor layers with the standardized manufacture process which is known conventionally to the stoichiometry, it is an easy manufacturing process and the manufacture method of this invention can manufacture a complementary-type semiconductor device more nearly high-speed than a silicon complementary-type semiconductor device with sufficient repeatability
[0022]
[Example] Drawing 3 or drawing 9 is drawing explaining the manufacturing process of the example of this invention.
Drawing 3 (a) It is Si0.5 germanium0 5 first 3 **. Gray dead Si1-x Gex which the germanium composition x of 10nm increases from 0.5 on a substrate 11 1.0 Gray dead Si1-y Gey to which the germanium active layer 13 and the germanium composition y of 30nm of 12 or 30nm of layers decrease

from 1.0 to 0.5 A layer 14 is made to deposit by the molecular-beam epitaxial grown method (the MBE method) one by one. In this case, gray dead Si1-x Gex A layer 12 acts as a buffer layer which eases a substrate 1 and the grid mismatching of germanium active-layer 13 grade established on it.

[0023] In addition, germanium composition ratio of a substrate 11 is gray dead Si1-x Gex that not to be restricted to 0.5 and what is necessary is just the range of 0.3 or 0.7. What is necessary is just the thickness 0 or the range of 100nm that what is necessary is just to make it change of the composition x of a layer 12 also increase from the composition ratio of a substrate 11 to the composition ratio of an active layer 13. Moreover, the germanium active layer 13 is gray dead Si1-y Gey further that what is necessary is just less than thickness sufficient [that germanium composition should just be 90% or more of silicon germanium], i.e., 100nm, for the thickness to also form an active layer. The thickness should just also be 100nm or less that germanium composition of the germanium active layer 13 of a layer 14 and the front face of an opposite side should just be 0.3 or 0.7.

[0024] Subsequently, after growing up the high resistance GaAs layer 15 using the MBE method which made growth temperature 250 degrees C, heat treatment is performed for 10 minutes at 600 degrees C. When growing up a III-V group compound semiconductor at low temperature from such usual growth temperature Many [1 to 2%] semiconductor layers are obtained for V group element to a stoichiometry, and with subsequent heat treatment, superfluous V group elements gather granular and serve as a metal grain. Metal-semiconductor junction (Schottky barrier) is made to the circumference of a metal grain in a semiconductor layer, and a carrier depletion-izes and becomes high resistance (77 p. IEEE ELECTRON DEVICE[besides Smith] LETTERS, EDL9, 1988).

[0025] In the case of this GaAs layer 15, the GaAs-metal As Schottky barrier is formed, and the resistivity is 105-107. It becomes omega-cm and becomes the isolation layer which separates p type transistor and n type transistor electrically. In addition, what is necessary is for the thickness 100 or the range of the growth temperature of this GaAs layer just to be 500nm that what is necessary is just the range of 150 degrees C or 450 degrees C. Moreover, many [1 to 2%] of other III-V group compound semiconductor layers are sufficient as V group element to a stoichiometry, for example, in the case of an AlGaAs layer, this GaAs layer 15 becomes the resistivity of 1011 ohm-cm.

[0026] Subsequently, the n type aluminum0.3 Ga0.7As carrier supply layer 17 of 16 or 20nm of 50nm of high grade GaAs layers and the 10nm n type In0.3 Ga0.7 As ohmic-contact layer 18 are made to deposit by the MBE method. It sets at these deposition processes and is gray dead Si1-y Gey. Since a layer 14 acts as a counter diffusion prevention layer which prevents the counter diffusion of germanium, and Ga and As, the quality of the high grade GaAs layer 6 prepared on it can be kept quality.

[0027] In addition, that the thickness of the high grade GaAs layer 16 should just be about 100nm The range of aluminum composition ratio a of the n type aluminum0.3 Ga0.7 As carrier supply layer 17 is $0.0< a<=1.0$. And that the thickness should just be 40nm or less, the range of In composition ratio b of the n type In0.3 Ga0.7 As ohmic-contact layer 18 is $0.0<=b<=1.0$, and the thickness should just be about 100nm further.

[0028] Drawing 3 (b) Subsequently it is H3 PO4 3 **, using the photoresist pattern 19 as a mask. : H2 O2 : Etching removal of the n type In0.3 Ga0.7As ohmic-contact layer 18 or the high resistance GaAs layer 15 is alternatively carried out using the phosphoric-acid system etching reagent of H2 O=1:1:25.

[0029] Drawing 4 (c) 3 **, subsequently, after removing a photoresist pattern, by applying and carrying out patterning of the new photoresist, the 2nd photoresist pattern 20 is formed, the ion implantation of the oxygen ion is carried out by the dose of 1x1015cm-2 by using this photoresist pattern 20 as a mask, and the isolation field 21 is formed.

[0030] Drawing 4 (d) 3 **. subsequently, after removing a photoresist pattern, the silicon nitriding oxide film (SiON film) 22 is made to deposit on the whole surface by the plasma CVD method, and the 3rd photoresist pattern 23 which has opening corresponding to the gate section of p type IGFET by applying and carrying out patterning of the photoresist is formed.

[0031] Drawing 5 (e) Subsequently it is CF4 3 **, using the 3rd photoresist pattern as a mask. 3.9% of O2 CF4 which consists of gas By the dry etching using system gas, they are the silicon nitriding oxide

film 22 and gray dead Si1-y Gey. A layer 14 is removed alternatively and the germanium active layer 13 is exposed.

[0032] Drawing 5 (f) Subsequently it is O2 3 **, using the silicon nitriding oxide film 22 as a mask. : By heat-treating for 20 minutes at the substrate temperature of 550 degrees C in the atmosphere of N 2 = 1:3 Nitriding and oxidization are performed simultaneously and they are the germanium active layer 13 and gray dead Si1-y Gey. The gate insulator layer 24 which consists of a nitriding oxide (germanium2 N2 O) with a thickness of 10nm is formed in the exposure front face of a layer 14. (In addition about this nitriding / oxidization process, they are Journal of Electrochemical Society, vol.135-4, p.961, and 1988 references.)

In addition, what is necessary is for 3 or the range of the thickness of this gate insulator layer 24 just to be 50nm.

[0033] Drawing 6 (g) Subsequently to the whole surface, the Cr/Au layer 25 which carries out the vacuum evaporationo of Cr and the Au, and serves as a gate electrode of p type IGFET is formed 3 **.

[0034] Drawing 6 (h) subsequently 3 ** by removing the silicon nitriding oxide film 22 by the fluoric acid system etching reagent of HF:H2 O=1:20 After carrying out the lift off of the Cr/Au layer 25 on the silicon nitriding oxide film 22 and forming the gate electrode 26, The 2nd silicon nitriding oxide film 27 is made to newly deposit on the whole surface by the plasma CVD method. It is CF4, using a photoresist (not shown) as a mask. The dry etching using system gas removes the 2nd silicon nitriding oxide film 27 on the source drain formation field of p type IGFET, and the gate electrode 26.

[0035] Drawing 7 (i) It is p+ by, carrying out the 2nd silicon nitriding oxide film 27 subsequently to a mask 3 **, carrying out the ion implantation of the B (boron) of dose 2x1014cm-2, and heat-treating at the temperature of 350 degrees C. The type source drain fields 28 and 29 are formed.

[0036] Drawing 7 (j) 3 **, subsequently to the whole surface, after forming the 4th photoresist pattern 30 which has opening for source drain electrode formation by applying and carrying out patterning of the photoresist, the Pd/Cr/Au layer 31 which carries out the vacuum evaporationo of Pd (palladium), Cr, and the Au, and serves as a source drain electrode is formed.

[0037] Drawing 8 (k) 3 **, subsequently, after carrying out the lift off of the Pd/Cr/Au layer on the 4th photoresist pattern and forming the source drain electrodes 32 and 33 by removing the 4th photoresist pattern, the 5th photoresist pattern 34 which has opening for gate electrode formation of n type HEMT is formed by applying and carrying out patterning of the photoresist to the whole surface.

[0038] And after carrying out etching removal of the 2nd silicon nitriding oxide film 27 and the n type In0.3 Ga0.7 As ohmic-contact layer 18 by having used this 5th photoresist pattern 34 as the mask and exposing the n type aluminum0.3 Ga0.7 As carrier supply layer 17, the vacuum evaporationo of the aluminum layer 35 used as the gate electrode of n type HEMT is carried out to the whole surface.

[0039] Drawing 8 (l) subsequently by removing the 5th photoresist pattern 3 ** By applying a photoresist to the whole surface and newly, carrying out patterning, after carrying out the lift off of the aluminum layer on the 5th photoresist pattern and forming the gate electrode 36 of n type HEMT The 6th photoresist pattern 37 which has opening for source drain electrode formation of n type HEMT is formed, and the Au-germanium/nickel/Au layer 38 which carries out the vacuum evaporationo of Au-germanium, and nickel and Au, and serves as a source drain electrode subsequently to the whole surface is formed.

[0040] drawing 9 -- by removing the 6th photoresist pattern subsequently 3 ** After carrying out the lift off of the Au-germanium/nickel/Au layer on the 6th photoresist pattern and forming the source drain electrodes 39 and 40, by performing heat treatment for 10 minutes at the substrate temperature of 450 degrees C The ohmic nature of the source drain electrodes 32, 33, 39, and 40 is raised, and the semiconductor device of a complementary type which consists of p type germanium IGFET and n type GaAsHEMT is completed In addition, what is necessary is for the range of the heat treatment temperature in this case just to be 400 degrees C or 450 degrees C.

[0041] In addition, in the above-mentioned example, although n type HEMT is used as an n type transistor, it is not restricted to this, and GaAsMESFET (Schottky barrier gate type field-effect

transistor) may not be used, the material of n type transistor is not restricted to GaAs, either, and other III-V group compound semiconductors with high electron mobility may be used.

[0042]

[Effect of the Invention] According to this invention, as a growth substrate in which germanium composition forms 90% or more of p-type-silicon germanium transistor, and an n type III-V group compound semiconductor transistor By making the gray dead silicon germanium layer in which germanium composition decreases between the active layer of p type transistor, and the active layer of n type transistor intervene using a silicon germanium substrate Since misfit transition and counter diffusion were suppressed, a quality semiconductor active layer can be obtained and the semiconductor device containing the complementary circuit which was excellent in the high-speed property with it can be manufactured with the sufficient manufacture yield.

[Translation done.]